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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LAM, CATHY N	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/572,655	EISERT ET AL.	
	Examiner	Art Unit	
	CATHY N. LAM	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-8,10-18 and 44-75* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8,10-18 and 44-75* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/19/2011*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 07/28/2011 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 10 is recites the limitation “the height (h1) in line 1, and "the distance (h2), in line 2. There is insufficient antecedent basis for this limitation in the claim.

4. Claim 11 is recites the limitation “the height (h1) in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 4-8, 44-47, 49-51, 61-64, 67-70, 73-75, are rejected under 35 U.S.C. 102(b) as being anticipated by Baur et al. (US 2004/0046179).

Regarding claim 1, Baur discloses in figure 5 a radiation emitting thin film semiconductor chip comprising:

an epitaxial multilayer structure 2 [0076] fig. 5 comprising:

an active, radiation-generating layer 3 [0060]

a first main face 5 [0060] and

a second main face 6 [0060] remote from the first main face for coupling out radiation generating in the active radiation generating layer, and

a reflective layer 10 [0074] or interface, and

wherein the first main face of the multilayer structure is coupled to the reflective layer 10 or interface, and

wherein a patterned region of the multilayer structure that adjoins the second main face of the multilayer structure is patterned by either one or two dimensional depressions forming convex elevations figs.1-2, fig.5, each said convex elevation having an upper surface that is not contiguous with an upper surface of an adjacent elevation fig.5.

Regarding claim 46, Baur discloses a radiation-emitting thin-film semiconductor chip comprising an epitaxial multilayer structure 2 figs. 1-2, fig.5 and a reflective layer 10 or interface, the epitaxial multilayer structure comprising:

an active, radiation-generating layer 3,

a first main face 5 and

a second main face 6 remote from the first main face for coupling out the radiation generated in the active, radiation-generating layer,

wherein the first main face of the multilayer structure is coupled to the reflective layer 10 or interface, and

wherein a patterned region of the multilayer structure that adjoins the second main face of the multilayer structure is patterned by either one- or two dimensional depressions forming convex elevations figs.1-2, fig.5, , each said convex elevation having an upper surface that is not contiguous with an upper surface of an adjacent elevation fig.5.

Regarding claims 4, 5, 49, 50, Baur discloses the semiconductor chip as claims 1, 46, wherein the elevations have a form of truncated pyramids or truncated cones or a trapezoidal cross sectional form or a form of cones or a triangular cross-section form fig.5.

Regarding claim 6, Baur discloses the semiconductor chip as claimed in claim 1, wherein the elevations have a form sphere segment or a circle segment cross sectional form [0031].

Regarding claims 7, 8, 51, 75, Baur discloses the semiconductor chip as claimed in claim 1, wherein the elevations have an inclination angle (ß) of between approximately 30° and approximately 70° (claim 6).

Regarding claim 44, Baur discloses the semiconductor chip as claimed in claim 1, wherein each of the convex elevations is defined by two-dimensional depressions fig.1.

Regarding claims 45, 47, Baur discloses the semiconductor chip as claimed in claim 1, wherein the epitaxial multilayer 2 of the semiconductor chip is free of a growth substrate fig.5.

Regarding claim 61, Baur discloses the semiconductor chip as claimed in claim 46, wherein the multilayer structure comprises a material or a plurality of different materials based on GaN [0034].

Regarding claim 62, Baur discloses the semiconductor chip as claimed in claim 1, wherein the second main face is a noncontinuous layer fig.5.

Regarding claim 63, Baur discloses the semiconductor chip as claimed in claim 1, wherein the reflective layer 10 is in direct contact with the epitaxial multilayer structure 2, fig.5.

Regarding claim 64, Baur discloses the semiconductor chip as claimed in claim 1, wherein the epitaxial multilayer structure is based on a II-VI semiconductor material (GaN, [0034]).

Regarding claim 67, 73, Baur discloses the semiconductor chip as claimed in claim 1, wherein the patterned region of the multilayer structure that adjoins the second

main face of the multilayer structure is patterned by two-dimensional depressions forming convex elevations figs.1-2,5.

Regarding claim 68, Baur discloses the semiconductor chip as claimed in claim 46, wherein the second main face is a noncontinuous layer, fig.5.

Regarding claim 69, Baur discloses the semiconductor chip as claimed in claim 46, wherein the reflective layer 10 is in direct contact with the epitaxial multilayer structure fig.5.

Regarding claim 70, Baur discloses the semiconductor chip as claimed in claim 46, wherein the epitaxial multilayer structure is based on a II-VI semiconductor material (GaN, [0034]).

Regarding claim 74, Baur discloses the semiconductor chip as claimed in claim 1, wherein the convex elevations have a height (hl) at least as large as a distance (h2) between the patterned region and the active, radiation-generating layer figs.1-2.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims, 2, 10-18, 48, 52-60, are rejected under 35 U.S.C. 103(a) as being unpatentable over Baur et al. (US 2004/0046179).

Regarding claims 2, 48, Baur discloses the semiconductor chip as claimed in claims 1, 46.

Baur does not disclose in the fifth embodiment of fig. 5 that a carrier element coupled to the first main face, wherein the reflective layer 10 or interface is arranged between the carrier element and the multilayer structure.

Baur discloses in the seventh embodiment of fig.7 that a carrier element 12 [0079] coupled to the first main face, wherein the reflective layer 10 or interface is arranged between the carrier element 12 and the multilayer structure 2, fig.7.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a carrier element coupled to the first main face, wherein the reflective layer or interface is arranged between the carrier element and the multilayer structure, in order to have heat dissipation and for contact connection [0079].

Regarding claims 10, **52**, **53**, Lester discloses the semiconductor chip as claimed in claims 1, 46.

Baur does not disclose the height (h1) of the elevations being approximately as large as or twice as large as the distance (h2) between the patterned region of the multilayer structure and the active, radiation generating layer.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made, to modify Baur by including the height of the elevations being approximately twice as large as the distance between the non patterned region of the multilayer structure and the active, radiation generating layer and the elevation, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claims 11, 54, Baur discloses the transistor chip as claimed in claims 1, 46, the elevations have a light emitted opening dimension.

Baur does not disclose the cell size (d) of the elevations being at most approximately five times as large as the height (h1)of the elevations.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify Baur by including a light emitted opening dimension of the elevations being at most approximately five times as large as the height of the elevations, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272,205 USPQ 215 (CCPA 1980).

Regarding claims 12, **55**, Baur discloses the transistor chip as claimed in claims 1, 46, the elevations have a light emitted opening dimension.

Baure does not disclose the cell size of the elevations being at most approximately three times as large as the height of the elevations.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made, to modify Baur by including the light emitted opening

dimension of the elevations being at most approximately three times as large as the height of the elevations, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claims 13, **14, 56,** Baure discloses the transistor chip as claimed in claims 1, 46.

Baur does not disclose the reflective layer or interface coupled to the first main area of the multilayer structure has a reflection at least 70%, and a reflectivity of at least 85%.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made, to modify Baur by including the reflective layer or interface coupled to the first main area of the multilayer structure has a reflection at least 70%, and a reflectivity of at least 85%, in order to improve the performance of the device. Since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claims 15, 57, Baur discloses the transistor chip as claimed in claim 1.

Baur does not disclose in the fifth embodiment of fig.5 the multilayer structure is applied on a carrier substrate either directly by its first main face or via a reflective layer.

Baur discloses in the seventh embodiment of fig. 7 the multilayer structure 2 is applied on a carrier substrate 12 fig.7 either directly by its first main face or via a reflective layer 10.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the multilayer structure is applied on a carrier substrate either directly by its first main face or via a reflective layer in order to have heat dissipation and for contact connection [0079].

Regarding claims 16, **58**, Baur discloses the transistor chip as claimed in claim 15,wherein the reflective layer 10 or the carrier substrate serves as a contact layer of the semiconductor component [0074].

Regarding claims 17, 18, 59-60, Baur discloses the transistor chip as claimed in claim 1.

Baur does not disclose in the fifth embodiment of fig.5 a conductive transparent layer applied onto the second main face of the multilayer structure.

Baur discloses in the seventh embodiment of fig. 7 a conductive transparent layer 13 applied onto the second main face of the multilayer structure.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a conductive transparent layer applied onto the second main face of the multilayer structure, in order to protect the device.

2. Claims, 65-66, 71-72, are rejected under 35 U.S.C. 103(a) as being unpatentable over Baur et al. (US 2004/0046179) in view of Lester (U.S. Patent No. 6,291,839).

Regarding claims 65, 71, Baur discloses the semiconductor chip as claimed in claims 1, 46.

Baur does not disclose the epitaxial multilayer structure is based on a phosphide compound semiconductor material.

Lester discloses the epitaxial multilayer structure is based on a phosphide compound semiconductor material (col.5 line 20).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the epitaxial multilayer structure is based on a phosphide compound semiconductor material, in order to improve the performance of the device.

Regarding claims 66, 72, Baur discloses the semiconductor chip as claimed in claims 1, 46.

Baur does not disclose the epitaxial multilayer structure is based on an arsenide compound semiconductor material.

Lester discloses the epitaxial multilayer structure is based on an arsenide compound semiconductor material (col.5 line 20).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the epitaxial multilayer structure is based on an arsenide compound semiconductor material, in order to improve the performance of the device.

Response to Arguments

Applicant's arguments with respect to claims 1-2, 4-8, 10-18, 44-75, have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CATHY N. LAM whose telephone number is (571)270-5021. The examiner can normally be reached on M-F 7:30AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, LYNNE GURLEY can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CL
10/11/2011

/CUONG Q NGUYEN/

Primary Examiner, Art Unit 2811